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Ćw. 4

Timery

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Cel ćwiczenia

Celem ćwiczenia jest opracowanie programu wykorzystującego przerwania od układów czasowych mikrokontrolera ADuC842.

Zagadnienia do przygotowania:

- Budowa i działanie liczników/timerów w układzie ADuC 842.
- Wektor przerwań.
- Obsługa przerwań od timerów w języku asemblera.
- Elementy języka asemblera poznane dotychczas na zajęciach.

Wprowadzenie

Mikrokontroler 842 posiada 4 wbudowane układy, które mogą pracować niezależnie, jako układy odliczające czas timers lub zliczające impulsy liczniki. Trzy z nich Timero, Timer1 i Timer2 można zastosować w sposób dowolny. Timer3 został wbudowany do taktowania portu szeregowego. Timery programowane są za pomocą dwóch rejestrów TMOD (timer mode - *Tab.1*) i TCON (timer control – *Tab.2*). Trzeci z timerów - T2 stanowi dla mikrokontrolera układ, którego tryb pracy jest ustalany w rejestrze T2CON – *Tab.3*. T2 jest licznikiem 16 bitowym z dodatkową parą rejestrów roboczych RCAP2H i RCAP2L, służących do przeładowywania lub zapisu aktualnej wartości licznika T2.

Podstawą układów odliczania czasu i zliczania impulsów są dwa liczniki TL0 (młodsza część) i TH0 (starsza część) dla układu Timer0 oraz TL1 i TH1 dla układu Timer1.

Aby uruchomić układy T0, T1 należy zdecydować czy mają one pracować, jako timery czy jako liczniki (C/T = „0” – timer). Następnie wyznaczyć moment startu zliczania TR0/1 RUN.

Table 28. TMOD SFR Bit Designations

Bit No.	Name	Description
7	Gate	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. Cleared by software to enable Timer 1 whenever the TR1 control bit is set.
6	C/T	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (Used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.
2	C/T	Timer 0 Timer or Counter Select Bit. Set by software to select counter operation (input from T0 pin). Cleared by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

Tab.1

Table 29. TCON SFR Bit Designations

Bit No.	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	IE1[1]	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{INT1}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
2	IT1[1]	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection, i.e., 1-to-0 transition. Cleared by software to specify level-sensitive detection, i.e., zero level.
1	IE0[1]	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or by a zero level being applied to external interrupt pin $\overline{INT0}$, depending on the state of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
0	IT0[1]	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection, i.e.,1-to-0 transition. Cleared by software to specify level-sensitive detection, i.e., zero level.

[1]These bits are not used in the control of Timer/Counter 0 and 1, but are used instead in the control and monitoring of the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Tab.2

Table 30. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Tab.3

Zadania

- ***Napisać program, który będzie na 4 segmentach wyświetlacza LED odmierzał czas minut i sekund. Do odmierzania czasu (1 sekundy) wykorzystać jeden z timerów i przerwania od niego. Po wystartowaniu programu wszystkie segmenty mają wskazywać zero. Minuty i sekundy mają być rozdzielone kropką.***

Literatura

- http://www.analog.com/media/en/technical-documentation/data-sheets/ADUC841_842_843.pdf
- Andrzej Radzewski: *Mikrokomputery jednoukładowe rodziny MCS'51*, WNT 1992,